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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/039,580	Applicant(s) DAVID, HOWARD S.	
	Examiner Zhuo H Li	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,11-16 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,11-16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in respond to the amendment filed on December 31, 2003 (Paper No. 5).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 and 3-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, the newly amended limitation "the command sequencer and serializer unit to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a point-to-point interconnect between the command sequencer and serializer unit and the memory module" is neither clearly disclosed in the drawing nor described in the specification. If applicant believe it does disclosed in at the time the application was filed, please point it out to the examiner with the detail page and line numbers in the response.

Regarding claims 3-7 are also rejected because of depending on claim 1, containing the same deficiency.

The following art rejections are applied from what is best understood of the claim(s) in view of the 112 First paragraph problems listed above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 8, 15-16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,718 hereinafter Stracovsky) in view of Yoo et al. (2002/012, 921, 5 hereinafter Yoo).

Regarding claim 1, Stracovsky discloses an apparatus (100, figure 1B) comprising a an array of tag address storage locations, i.e., resources tag (114, figure 1B), a command sequencer and serializer unit, i.e., command sequencer (116, figure 1B) couple to the array of tag address locations (figure 1B), the command sequencer unit to control a memory module, i.e., shared resources memory (108, figure 1B) via the sequenced universal command bus (220, figure 1B), the command sequencer to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a point-to-point interconnect between the command sequencer and serializer unit

and the memory module, i.e., the command sequencer is one of the component located in the universal controller as define in figure 1B, wherein the universal controller is able to received the requested commands and data signals from a plurality of processors (102, figure 1D) via the system bus (106, figure 1D), and further transfer the requested to the shared memory via the sequenced universal command (220, figure 1D), in addition, the universal controller having a system interface (110 figure 1D) arranges to covert the received system command and system address from the multiple processors, and further compares with a look up table in communicate with the resource tags, and comparator (122, figure 1D), further transfer the higher priority requested to the respective memory module via the unidirectional command bus (912, figure 9A) and bi-directional data bus (914, figure 9A) in order to avoid data collisions or other type conflicts (col. 5 line 49 through col. 8 line 64 and col. 9 lines 2-15). Stracovsky differs from the claimed invention in not specifically teaches a data cache located on a memory module, and command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache. However, Yoo teaches the computer system in figure 1, comprising a memory controller (40, figure 1) generate memory requested to accessing the memory modules (42A and 42B, figure 1) wherein each of the memory module comprising a plurality of DRAM (44, figure 1) and data queue buffer (48, figure 1) and a command address buffer wherein the memory controller performing a point-to-point interconnect between the memory module by a plurality of command and address buses (56, figure 1), and the memory module generates a memory read clock signal in response to the first write clock signal for reading data from the memory to the buffer, i.e., data cache, if the read command indicates that the data is to be read from the memory

in the module (P0017 lines 12-27 and P0037 through P0038). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, and command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache, as per teaching by the system of Yoo, because it utilizing the maximum operable data transmission rate by ensures the dame phase relationship for the write clock in the write direction for all data transfers between modules, and the read clock in the read direction for all data transfers between modules, regardless the module location.

Regarding claim 3, Yoo discloses the command sequencer and serializer to deliver a read and pre-load command to the data cache located on the memory module, the read and pre-load command to cause the current line of data to be read out of the memory mould memory device and to load the next line of data from the memory module memory device to the data cache (P0017 lines 12-27 and P0037 through P0038).

Regarding claim 8, Stracovsky discloses a memory module (108, figure 1B), comprising at least one memory device (device type 1 – device type N, figure 1C), and the memory controlled by a plurality of commands delivered by a memory controller, i.e., universal controller (104, figure 1B) via a memory bus (220, figure 1B), the memory controller component including an array of tag address storage locations, i.e., resource tags (114, figure 1B). Stracovsky differs from the claimed invention in not specifically teaches the memory module comprising at data cache coupled to the memory device, the plurality of commands including a read and pre-load command to cause a current line data to be read out of the memory device and to load a next line

of data from the memory device to the data cache. However, Yoo teaches the computer system in figure 1, comprising a memory controller (40, figure 1) generate memory requested to accessing the memory modules (42A and 42B, figure 1) wherein each of the memory module comprising a plurality of DRAM (44, figure 1) and data queue buffer (48, figure 1) and a command address buffer wherein the memory controller performing a point-to-point interconnect between the memory module by a plurality of command and address buses (56, figure 1), and the memory module generates a memory read clock signal in response to the first write clock signal for reading data from the memory to the buffer, i.e., data cache, if the read command indicates that the data is to be read from the memory in the module (P0017 lines 12-27 and P0037 through P0038). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, and command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache, as per teaching by the system of Yoo, because it utilizing the maximum operable data transmission rate by ensures the dame phase relationship for the write clock in the write direction for all data transfers between modules, and the read clock in the read direction for all data transfers between modules, regardless the module location.

Regarding claim 15, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller, i.e., universal controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B) he memory controller including an array of tag address storage locations (114, figure 1B), and command sequencer and serializer

unit (116, figure 1B) coupled to the array of tag address storage locations as defined in figure 1, a memory module (108, figure 1B) coupled to the memory controller via a memory bus (220, figure 1B), the memory module including at least one memory device (device type 1 – device type N, figure 1C). Straocvsky differs from the claimed invention in not specifically teaches the memory module comprising at data cache coupled to the memory device, the plurality of commands including a read and pre-load command to cause a current line data to be read out of the memory device and to load a next line of data from the memory device to the data cache. However, Yoo teaches the computer system in figure 1, comprising a memory controller (40, figure 1) generate memory requested to accessing the memory modules (42A and 42B, figure 1) wherein each of the memory module comprising a plurality of DRAM (44, figure 1) and data queue buffer (48, figure 1) and a command address buffer wherein the memory controller performing a point-to-point interconnect between the memory module by a plurality of command and address buses (56, figure 1), and the memory module generates a memory read clock signal in response to the first write clock signal for reading data from the memory to the buffer, i.e., data cache, if the read command indicates that the data is to be read from the memory in the module (P0017 lines 12-27 and P0037 through P0038). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, and command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache, as per teaching by the system of Yoo, because it utilizing the maximum operable data transmission rate by ensures the dame phase relationship for the write clock in the write direction

for all data transfers between modules, and the read clock in the read direction for all data transfers between modules, regardless the module location.

Regarding claim 16, Yoo discloses the memory module further including a command decoder and de-serializer unit (46A or 46B, figure 1) to receive command and address information from the memory controller (40, figure 1), the command decoder and de-serializer unit providing controller for the data cache (PP0033 line 1 through PP0036 line 8).

Regarding claim 22, Yoo discloses the system further comprising a point-to-point interconnect to couple the memory controller (40, figure 1) to the memory modules (42A and 42B, figure 1) via the buses (56, figure 1) and (PP0017 line 1 through line 27 and PP0031 line 1 through line 13).

6. Claims 4-7, 11-14 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,718 hereinafter Stracovsky) and Yoo et al. (2002/012, 921, 5 hereinafter Yoo) as applied to claim 1 above, and further in view of Ayukawa et al. (US PAT. 6,381,671 hereinafter Ayukawa).

Regarding claim 4, the combination of Stracovsky and Yoo differs from the claimed invention in not specifically teaches the read and pre-load command including memory module destination information, way information, address strobe state information and cache hit information. However Ayukawa teaches such (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of the combination of Stracovsky and Yoo in having the read and pre-load command including memory module destination information, way

information, address strobe state information and cache hit information, as per teaching by the system of Aynkawa, because it enhances the hit ratio of the sense amplifier cache by next address self-prefetching, and enhances the speed of first access to a multi-bank memory.

Regarding claim 5, Ayukawa discloses the read and preload command further including column address information and memory device bank information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claims 6-7, Ayukawa discloses the read and preload command information delivered over four transfer periods, i.e., 6 to 8 clock cycles, and the cache hit information and way information transferred during the fourth transfer period (figure 6 and 7 and col. 13 line 47 through col. 15 line 4).

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claims 13-14, the limitations of the claims are rejected as the same reasons set forth in claims 6-7.

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claims 20-21, the limitations of the claims are rejected as the same reasons set forth in claims 6-7.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 3-8, 11-16 and 18-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

March 19, 2004

MATTHEW KIM
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